IN THE CLAIMS:

Claims 24 through 43 were previously cancelled. None of the claims have been amended herein. All of the pending claims 1 through 23 are presented below. This listing of claims will replace all prior versions and listings of claims in the application. Please enter these claims as previously amended.

Listing of Claims:

1. (Original) A method for dicing a semiconductor substrate, comprising:

at least partially severing the semiconductor substrate along a first street;

at least partially severing the semiconductor substrate along a second street that extends substantially the same direction as the first street and is spaced a first distance apart from the first street; and

at least partially severing the semiconductor substrate along a third street extending in substantially the same direction as the first and second streets, the third street spaced a second distance from the second street without another cut between the second and third streets, the second distance being different than the first distance.

2. (Original) The method of claim 1, further comprising forming a scribe line along the first street.

3. (Original) The method of claim 2, wherein the forming the scribe line precedes the at least partially severing the semiconductor substrate along the first street.

4. (Original) The method of claim 1, further comprising forming a scribe line along the second street.

5. (Original) The method of claim 4, wherein the forming the scribe line precedes the at least partially severing the semiconductor substrate along the second street.

6. (Original) The method of claim 1, further comprising forming a scribe line along the third street.

7. (Original) The method of claim 6, wherein the forming the scribe line precedes the at least partially severing the semiconductor substrate along the third street.

8. (Original) The method of claim 1, wherein the at least partially severing the semiconductor substrate along the first and second streets is effected substantially simultaneously.

9. (Original) The method of claim 8, wherein the at least partially severing the semiconductor substrate along the first and second streets is effected at a different time than the at least partially severing the semiconductor substrate along the third street.

10. (Original) The method of claim 9, wherein the at least partially severing the semiconductor substrate along the third street is effected independently of at least partially severing the semiconductor substrate at any other location.

11. (Original) The method of claim 1, further comprising repeating a sequence of the at least partially severing the semiconductor substrate along each of the first, second, and third streets.

12. (Original) The method of claim 1, further comprising at least partially severing the semiconductor substrate along another street spaced a third distance apart from an adjacent one of the first, second, or third streets.

13. (Original) The method of claim 1, wherein at least partially severing the semiconductor substrate along at least one of the first, second, and third streets comprises substantially severing the semiconductor substrate.

14. (Original) The method of claim 13, wherein at least partially severing the semiconductor substrate along each of the first, second, and third streets comprises substantially severing the semiconductor substrate.

15. (Original) A method for dicing a semiconductor substrate, comprising:
at least partially severing the semiconductor substrate at a first substantially linear location;
at least partially severing the semiconductor substrate at a second substantially linear location which extends in substantially the same direction as the first substantially linear location and is spaced a first distance apart from the first substantially linear location; and
at least partially severing the semiconductor substrate at a third substantially linear location extending in substantially the same direction as the first and second substantially linear locations and spaced apart from the second substantially linear location a second distance which is different from the first distance, no intervening sever that extends in substantially the same direction as the third substantially linear location being located between the second and third substantially linear locations.

16. (Original) The method of claim 15, wherein at least partially severing the semiconductor substrate at at least one of the first, second, and third substantially linear locations comprises substantially severing the semiconductor substrate.

17. (Original) The method of claim 16, wherein at least partially severing the semiconductor substrate at each of the first, second, and third substantially linear locations comprises substantially severing the semiconductor substrate.

18. (Previously presented) The method of claim 16, further comprising forming a scribe line at at least one location of the first, second, and third substantially linear locations prior to substantially severing the semiconductor substrate at the at least one location.

19. (Original) The method of claim 15, wherein at least partially severing the semiconductor substrate at the first substantially linear location and at least partially severing the semiconductor substrate at the second substantially linear location are effected substantially simultaneously.

20. (Original) The method of claim 19, wherein at least partially severing the semiconductor substrate at the third substantially linear location is effected at a different time than at least partially severing the semiconductor substrate at the first and second substantially linear locations.

21. (Original) The method of claim 20, wherein at least partially severing the semiconductor substrate at the third substantially linear location is effected independently of at least partially severing the semiconductor substrate at any other location.

22. (Original) The method of claim 15, further comprising repeating the substantially severing.

23. (Original) The method of claim 15, further comprising at least partially severing the semiconductor substrate at another substantially linear location spaced a third distance apart from an adjacent one of the first, second, and third substantially linear locations.

24.-43. (Cancelled)